Intel® E7230 Chipset Memory Controller Hub (MCH)

Thermal/Mechanical Design Guide

July 2005

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Revision History

Revision Number	Description	Revision Date
001	• Initial Release.	June 2005

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1 Introduction

As the complexity of computer systems increases, so do the power dissipation requirements. Care must be taken to ensure that the additional power is properly dissipated. Typical methods to improve heat dissipation include selective use of ducting, and/or passive heatsinks.

The goals of this document are to:

- Outline the thermal and mechanical operating limits and specifications for the Intel® E7230 chipset memory controller hub (MCH).
- Describe a reference thermal solution that meets the specification of the Intel® E7230 chipset MCH.

Properly designed thermal solutions provide adequate cooling to maintain the Intel E7230 chipset MCH die temperatures at or below thermal specifications. This is accomplished by providing a low local-ambient temperature, ensuring adequate local airflow, and minimizing the die to local-ambient thermal resistance. By maintaining the Intel E7230 chipset MCH die temperature at or below the specified limits, a system designer can ensure the proper functionality, performance, and reliability of the chipset. Operation outside the functional limits can degrade system performance and may cause permanent changes in the operating characteristics of the component.

The simplest and most cost effective method to improve the inherent system cooling characteristics is through careful chassis design and placement of fans, vents, and ducts. When additional cooling is required, component thermal solutions may be implemented in conjunction with system thermal solutions. The size of the fan or heatsink can be varied to balance size and space constraints with acoustic noise.

This document addresses thermal design and specifications for the Intel E7230 chipset MCH components only. For thermal design information on other chipset components, refer to the respective component datasheet. For the PXH, refer to the *Intel® 6700PXH 64-bit PCI Hub/ 6702PXH 64-bit PCI Hub (PXH/PXH-V) Thermal/Mechanical Design Guidelines*. For the ICH7, refer to the *Intel® I/O Controller Hub 7 (ICH7) Thermal Design Guidelines*.

Note: Unless otherwise specified, the term “MCH” refers to the Intel E7230 chipset MCH.

1.1 Definition of Terms

BGA	Ball grid array. A package type, defined by a resin-fiber substrate, onto which a die is mounted, bonded and encapsulated in molding compound. The primary electrical interface is an array of solder balls attached to the substrate opposite the die and molding compound.
BLT	Bond line thickness. Final settled thickness of the thermal interface material after installation of heatsink.
MCH	Memory controller hub. The chipset component that contains the processor interface, the memory interface, the PCI Express* interface and the DMI interface.
PXH	Intel® 6700PXH 64-bit PCI Hub. The chipset component that performs PCI bridging functions between the PCI Express interface and the PCI

	bus. It contains two PCI bus interfaces that can be independently configured to operate in PCI (33 or 66 MHz) or PCI-X* mode 1 (66, 100 or 133 MHz), for either 32- or 64-bit PCI devices.
PXH-V	Intel® 6702PXH 64-bit PCI Hub. The chipset component that performs PCI bridging functions between the PCI Express interface and the PCI Bus. It contains one PCI bus interface that can be configured to operate in PCI (33 or 66 MHz) or PCI-X mode 1 (66, 100 or 133 MHz).
T_{case_max}	Maximum die or IHS temperature allowed. This temperature is measured at the geometric center of the top of the package die or IHS.
T_{case_min}	Minimum die or IHS temperature allowed. This temperature is measured at the geometric center of the top of the package die or IHS.
TDP	Thermal design power. Thermal solutions should be designed to dissipate this target power level. TDP is not the maximum power that the chipset can dissipate.

1.2 Reference Documents

The reader of this specification should also be familiar with material and concepts presented in the following documents:

Document Title	Document Number / Location
Intel® I/O Controller Hub 7 (ICH7) Thermal Design Guidelines	
Intel® I/O Controller Hub 7 (ICH7) Datasheet	
Intel® E7320 Chipset Memory Controller Hub(MCH) Datasheet	
Intel® Pentium® D Processor 840, 830 and 820 Datasheet	
Intel® Pentium® D Processor and Intel® Pentium® Processor Extreme Edition 840 Thermal and Mechanical Design Guidelines	
Intel® Pentium® Processor Extreme Edition and Intel® Pentium® D Processor Specification Update	
BGA/OLGA Assembly Development Guide	Contact your Intel Field Sales Representative
Various system thermal design suggestions	http://www.formfactors.org

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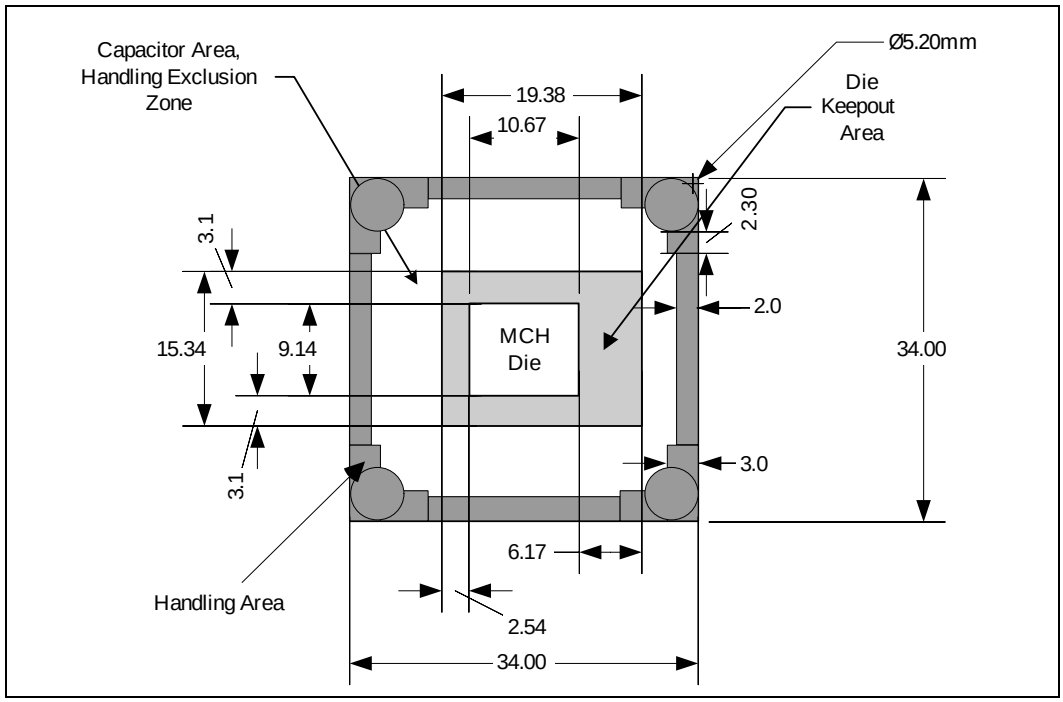
2 Packaging Technology

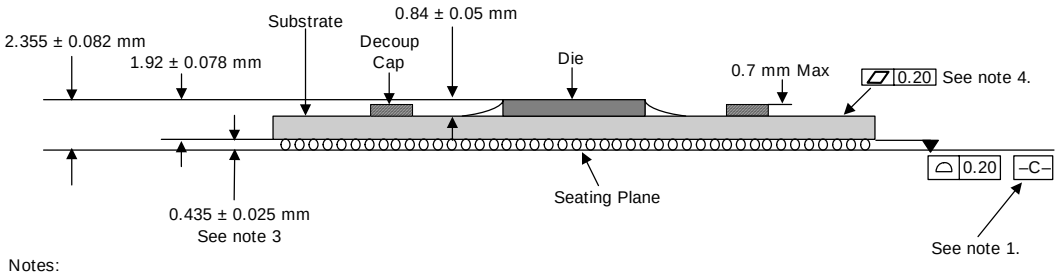
The Intel E7230 chipset consist of three individual components: the MCH, the ICH7 and the Intel 6700PXH 64-bit PCI Hub. The Intel E7230 chipset MCH components use a 34 mm squared, 6-layer flip chip ball grid array (FC-BGA) package (see Figure 2-1, Figure 2-2 and Figure 2-3). For information on the Intel 6700PXH 64-bit PCI Hub package, refer to the *Intel® 6700PXH 64-bit PCI Hub/6702PXH 64-bit PCI Hub (PXH/PXH-V) Thermal/Mechanical Design Guidelines*. For information on the Intel® I/O Controller Hub (ICH7) package, refer to the *Intel® I/O Controller Hub 7 (ICH7) Thermal Design Guidelines*.

Figure 2-1. MCH Package Dimensions (Top View)



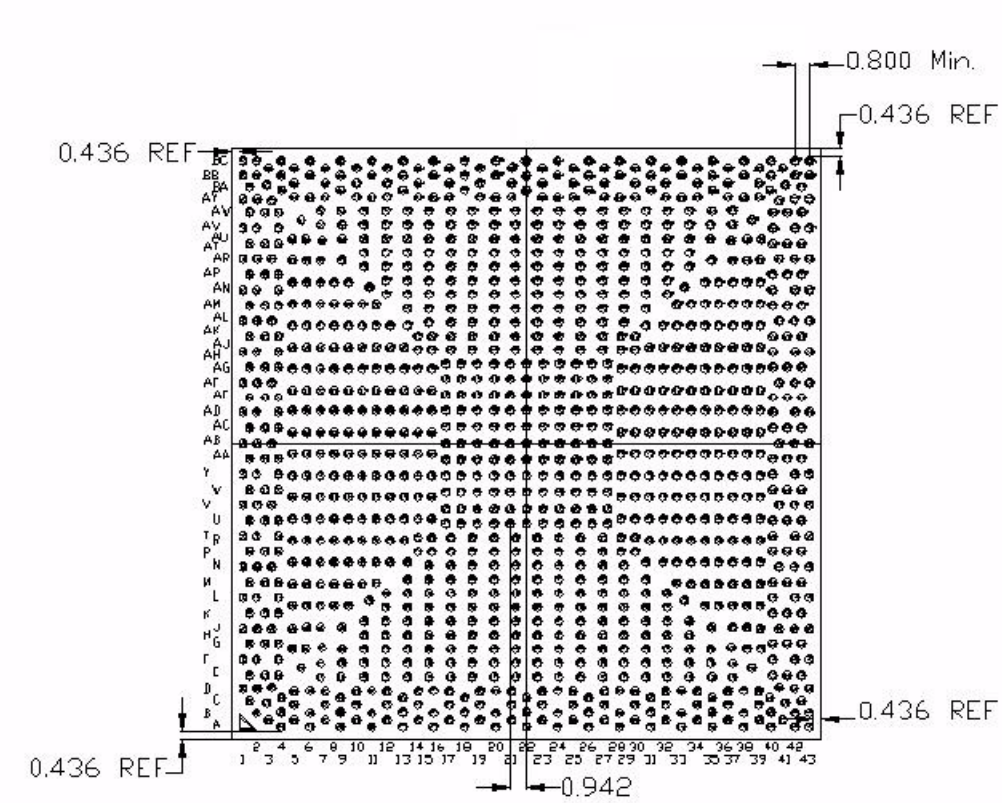
NOTE: All Dimensions are in millimeters.

Figure 2-2. MCH Package Dimensions (Side View)



Notes:
1. Primary datum -C- and seating plan are defined by the spherical crowns of the solder balls (shown before motherboard attach)
2. All dimensions and tolerances conform to ANSI Y14.5M-1994
3. BGA has a pre-SMT height of 0.5 mm and post-SMT height of 0.41-0.46 mm
4. Shown before motherboard attach; FCBGA has a convex (dome shaped) orientation before reflow and is expected to have a slightly concave (bowl shaped) orientation after reflow

Figure 2-3. MCH Package Dimensions (Bottom View)



NOTES:
1. All dimensions are in millimeters.
2. All dimensions and tolerances conform to ANSI Y14.5M-1994.

2.1 Package Mechanical Requirements

The Intel E7230 chipset MCH package has an exposed bare die which is capable of sustaining a maximum static normal load of 10 lbf. The package is NOT capable of sustaining a dynamic or static compressive load applied to any edge of the bare die. These mechanical load limits must not be exceeded during heatsink installation, mechanical stress testing, standard shipping conditions and/or any other use condition.

Notes:

1. The heatsink attach solutions must not include continuous stress onto the chipset package with the exception of a uniform load to maintain the heatsink-to-package thermal interface.
2. These specifications apply to uniform compressive loading in a direction perpendicular to the bare die top surface.
3. These specifications are based on limited testing for design characterization. Loading limits are for the package only.

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3 Thermal Specifications

3.1 Thermal Design Power (TDP)

Analysis indicates that real applications are unlikely to cause the MCH component to consume maximum power dissipation for sustained time periods. Therefore, in order to arrive at a more realistic power level for thermal design purposes, Intel characterizes power consumption based on known platform benchmark applications. The resulting power consumption is referred to as the Thermal Design Power (TDP). TDP is the target power level that the thermal solutions should be designed to. TDP is not the maximum power that the chipset can dissipate.

For TDP specifications, see Table 3-1 for the Intel E7230 chipset MCH. FC-BGA packages have poor heat transfer capability into the board and have minimal thermal capability without a thermal solution. Intel recommends that system designers plan for a heatsink when using the Intel E7230 chipset.

3.2 Die Case Temperature

To ensure proper operation and reliability of the Intel E7230 chipset MCH, the die temperatures must be at or between the maximum/minimum operating temperature ranges as specified in Table 3-1. System and/or component level thermal solutions are required to maintain these temperature specifications. Refer to Section 5 for guidelines on accurately measuring package die temperatures.

Table 3-1. Intel® E7230 Chipset MCH Thermal Specifications

Parameter	Value	Notes
T_{case_max}	105°C	
T_{case_min}	5°C	
$TDP_{dual\ channel}$	10.6 W	DDR2-533
$TDP_{dual\ channel}$	12.7 W	DDR2-667

Note: These specifications are based on silicon characterization; however, they may be updated as further data becomes available.

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4 Thermal Simulation

Intel provides thermal simulation models of the Intel E7230 chipset MCH and associated user's guides to aid system designers in simulating, analyzing, and optimizing their thermal solutions in an integrated, system-level environment. The models are for use with the commercially available Computational Fluid Dynamics (CFD)-based thermal analysis tool FLOTHERM* (version 5.1 or higher) by Flomerics, Inc. Contact your Intel field sales representative to order the thermal models and user's guides.

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5 Thermal Metrology

The system designer must make temperature measurements to accurately determine the thermal performance of the system. Intel has established guidelines for proper techniques to measure the MCH die temperatures. Section 5.1 provides guidelines on how to accurately measure the MCH die temperatures. Section 5.2 contains information on running an application program that will emulate anticipated maximum thermal design power. The flowchart in Figure 5-1 offers useful guidelines for thermal performance and evaluation.

5.1 Die Temperature Measurements

To ensure functionality and reliability, the T_{case} of the MCH must be maintained at or between the maximum/minimum operating range of the temperature specification as noted in Table 3-1. The surface temperature at the geometric center of the die corresponds to T_{case}. Measuring T_{case} requires special care to ensure an accurate temperature measurement.

Temperature differences between the temperature of a surface and the surrounding local ambient air can introduce errors in the measurements. The measurement errors could be due to a poor thermal contact between the thermocouple junction and the surface of the package, heat loss by radiation and/or convection, conduction through thermocouple leads, and/or contact between the thermocouple cement and the heatsink base (if a heatsink is used). For maximize measurement accuracy, only the 0° thermocouple attach approach is recommended.

5.1.1 Zero Degree Angle Attach Methodology

1. Mill a 3.3 mm (0.13 in.) diameter and 1.5 mm (0.06 in.) deep hole centered on the bottom of the heatsink base.
2. Mill a 1.3 mm (0.05 in.) wide and 0.5 mm (0.02 in.) deep slot from the centered hole to one edge of the heatsink. The slot should be parallel to the heatsink fins (see Figure 5-2).
3. Attach thermal interface material (TIM) to the bottom of the heatsink base.
4. Cut out portions of the TIM to make room for the thermocouple wire and bead. The cutouts should match the slot and hole milled into the heatsink base.
5. Attach a 36 gauge or smaller calibrated K-type thermocouple bead or junction to the center of the top surface of the die using a high thermal conductivity cement. During this step, ensure no contact is present between the thermocouple cement and the heatsink base because any contact will affect the thermocouple reading. **It is critical that the thermocouple bead makes contact with the die** (see Figure 5-3).
6. Attach heatsink assembly to the MCH and route thermocouple wires out through the milled slot.

Figure 5-1. Thermal Solution Decision Flowchart

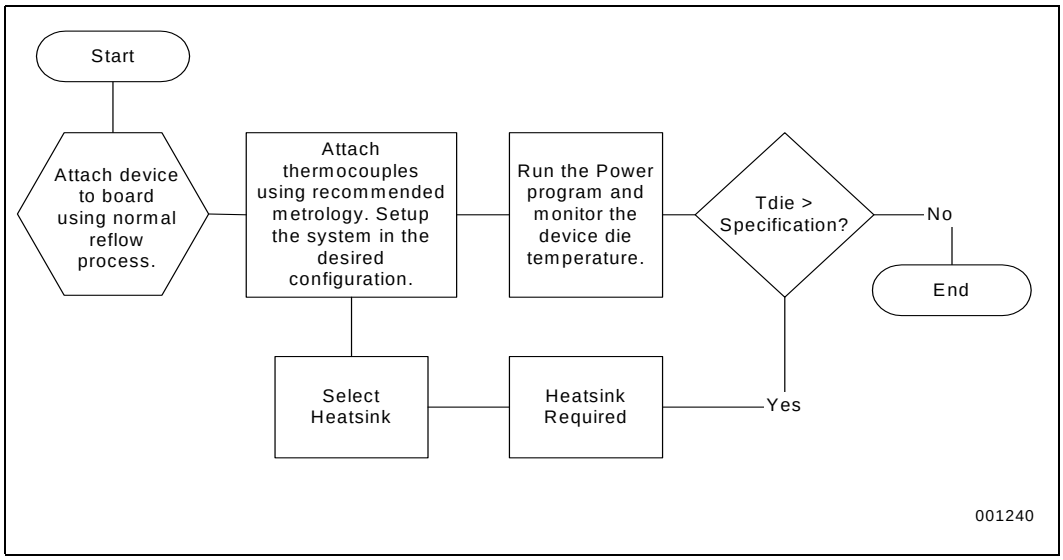
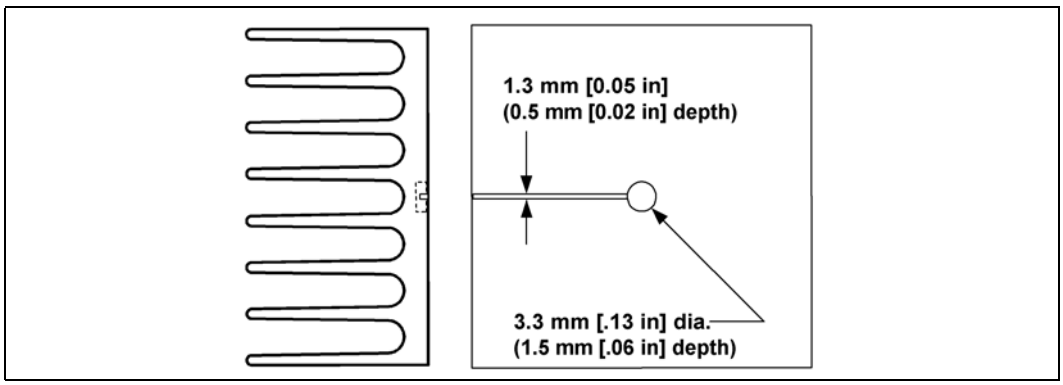
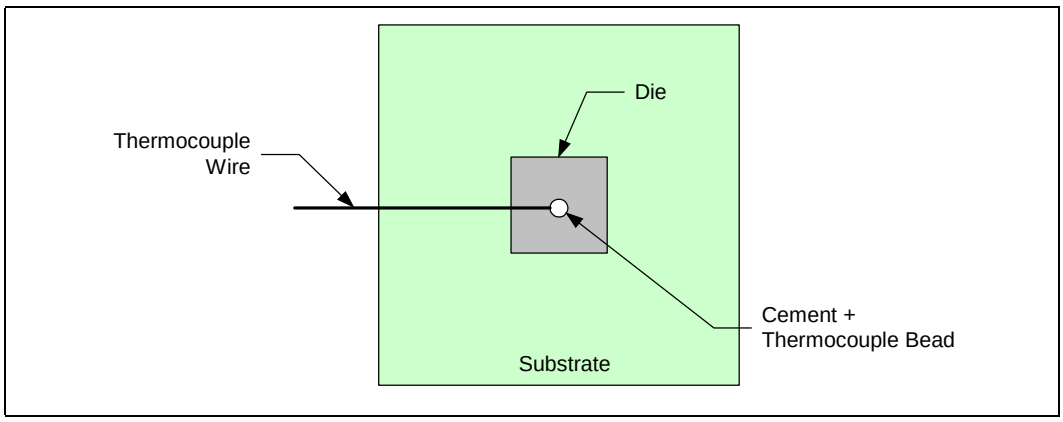


Figure 5-2. Zero Degree Angle Attach Heatsink Modifications



NOTE: Not to scale.

Figure 5-3. Zero Degree Angle Attach Methodology (Top View)



NOTE: Not to scale.

5.2 Power Simulation Software

The power simulation software is a utility designed to dissipate the thermal design power on an Intel E7230 chipset MCH when used in conjunction with the Prescott processor (1333 MHz). The combination of the above mentioned processor(s) and the higher bandwidth capability of the Intel E7230 chipset enable higher levels of system performance. To assess the thermal performance of the chipset MCH thermal solution under “worst-case realistic application” conditions, Intel is developing a software utility that operates the chipset at near worst-case thermal power dissipation.

The power simulation software being developed should only be used to test thermal solutions at or near the thermal design power. Figure 5-1 shows a decision flowchart for determining thermal solution needs. Real world applications may exceed the thermal design power limit for transient time periods. For power supply current requirements under these transient conditions, please refer to each component's datasheet for the ICC (Max Power Supply Current) specification. Contact your Intel field sales representative to order the power utility and user's guides.

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6 Reference Thermal Solution

Intel has developed a reference thermal solution to meet the cooling needs of the Intel® E7230 chipset MCH under operating environments and specifications defined in this document. This chapter describes the overall requirements for the Plastic Wave Soldering Heatsink (PWSH) reference thermal solution including critical-to-function dimensions, operating environment, and validation criteria. Other chipset components may or may not need attached thermal solutions, depending on your specific system local-ambient operating conditions. For information on the PXH family, refer to thermal specification in the *Intel® 6700PXH 64-bit PCI Hub/6702PXH 64-bit PCI Hub (PXH/PXH-V) Thermal/Mechanical Design Guidelines*. For information on the ICH7, refer to thermal specification in the *Intel® I/O Controller Hub 7 (ICH7) Thermal Design Guidelines*.

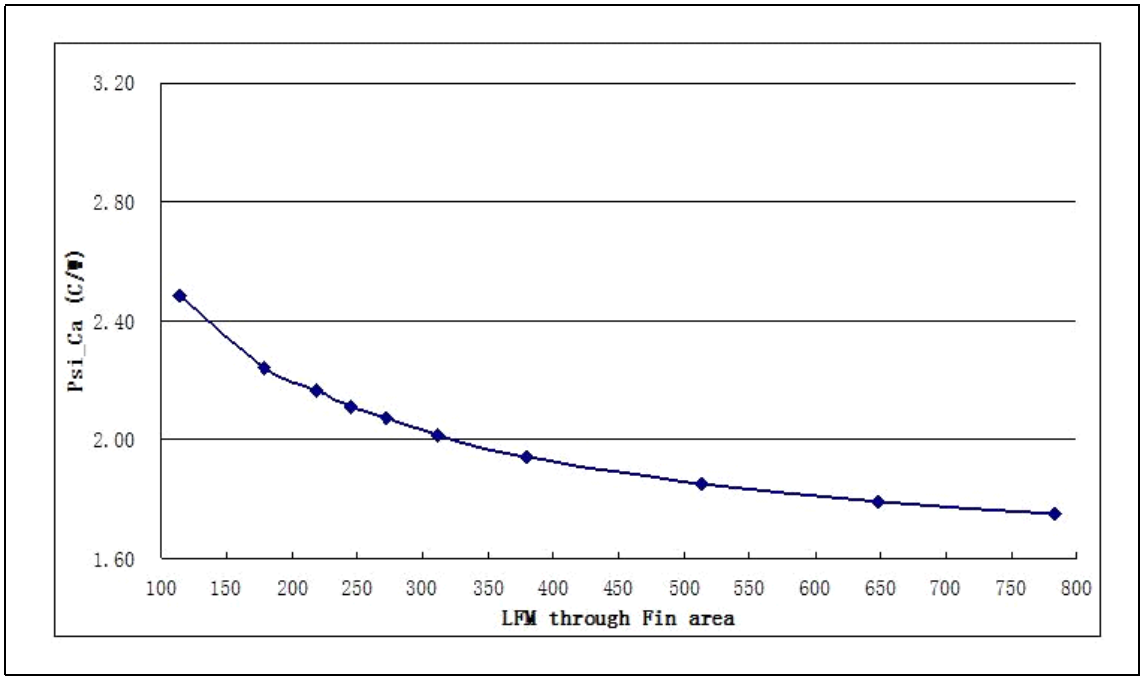
6.1 Operating Environment

The reference thermal solution was designed assuming a maximum local-ambient temperature of 55°C. The minimum recommended airflow velocity through the cross-section of the heatsink fins is 350 linear feet per minute (lfm) for 1U system and 450 linear feet per minute (lfm) for 2U+ system. The approaching airflow temperature is assumed to be equal to the local-ambient temperature. The thermal designer must carefully select the location to measure airflow to obtain an accurate estimate. These local-ambient conditions are based on a 35°C external-ambient temperature at sea level. (External-ambient refers to the environment external to the system.)

6.2 Heatsink Performance

Figure 6-1 depicts the measured thermal performance of the reference thermal solution versus approach air velocity. Since this data was measured at sea level, a correction factor would be required to estimate thermal performance at other altitudes.

Figure 6-1. Plastic Wave Soldering Heatsink Measured Thermal Performance versus Approach Velocity



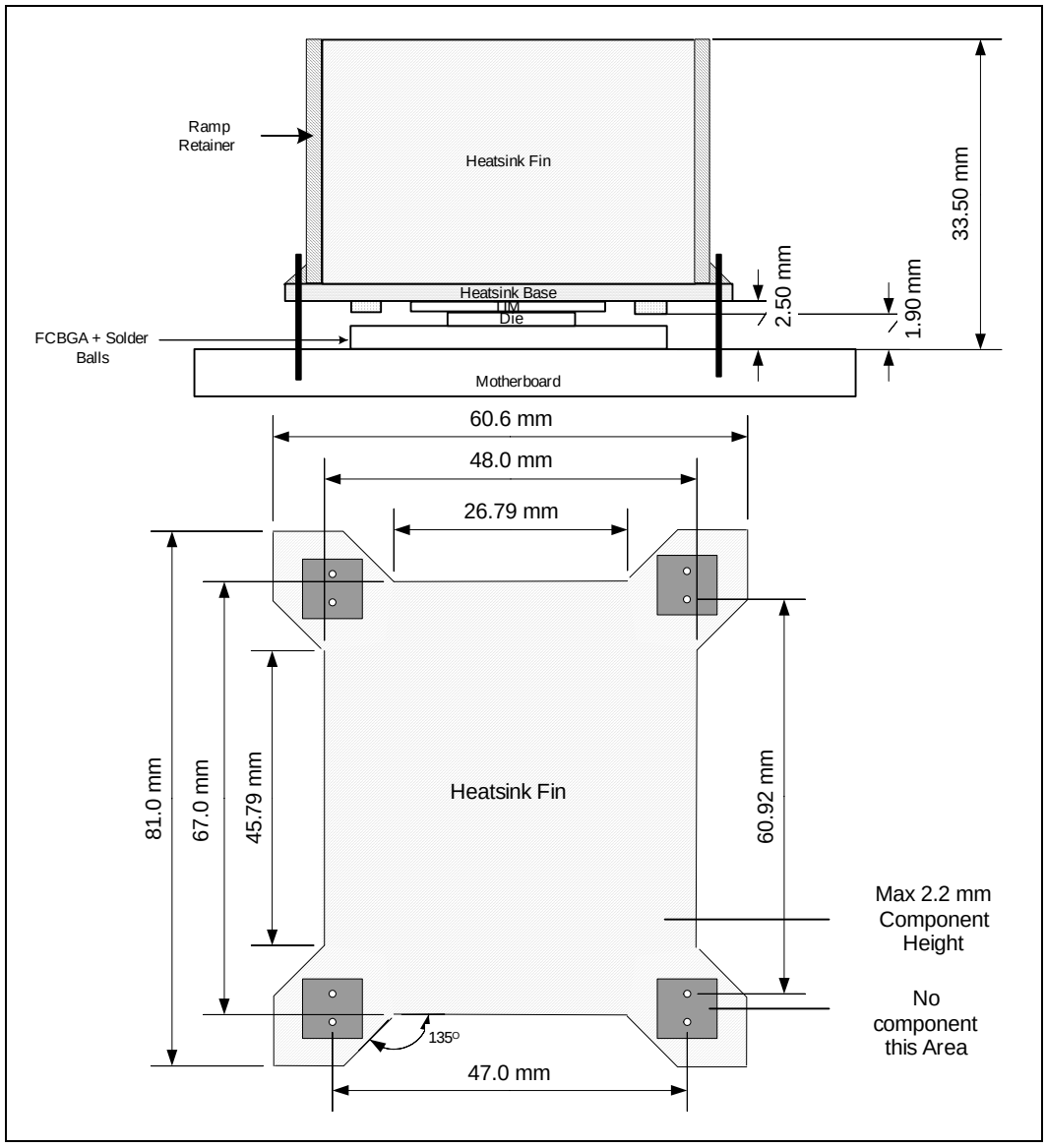
Note: Heatsink test result is based on End Of Line TIM performance, for worst case Heatsink performance with End of Life TIM, add +1.0C/W offset to Psi_ca.

6.3 Mechanical Design Envelope

While each design may have unique mechanical volume and height restrictions or implementation requirements, the height, width, and depth constraints typically placed on the Intel® E7230 chipset MCH thermal solution are shown in Figure 6-2.

When using heatsinks that extend beyond the chipset MCH reference heatsink envelope shown in Figure 6-2, any motherboard components placed between the heatsink and motherboard cannot exceed 2.19 mm (0.09 in.) in height.

Figure 6-2. Plastic Wave Soldering Heatsink Volumetric Envelope for the Chipset MCH



6.4 Board-Level Components Keepout Dimensions

The location of hole patterns and keepout zones for the reference thermal solution are shown in Figure 6-3 and Figure 6-4.

6.5 Plastic Wave Soldering Heatsink Thermal Solution Assembly

The reference thermal solution for the chipset MCH is a passive extruded heatsink with thermal interface. It is attached using a clip with each end hooked through an anchor soldered to the board. Figure 6-5 shows the reference thermal solution assembly and associated components.

Full mechanical drawings of the thermal solution assembly and the heatsink clip are provided in Appendix B. Appendix A contains vendor information for each thermal solution component.

Figure 6-3. Plastic Wave Soldering Heatsink Board Component Keepout

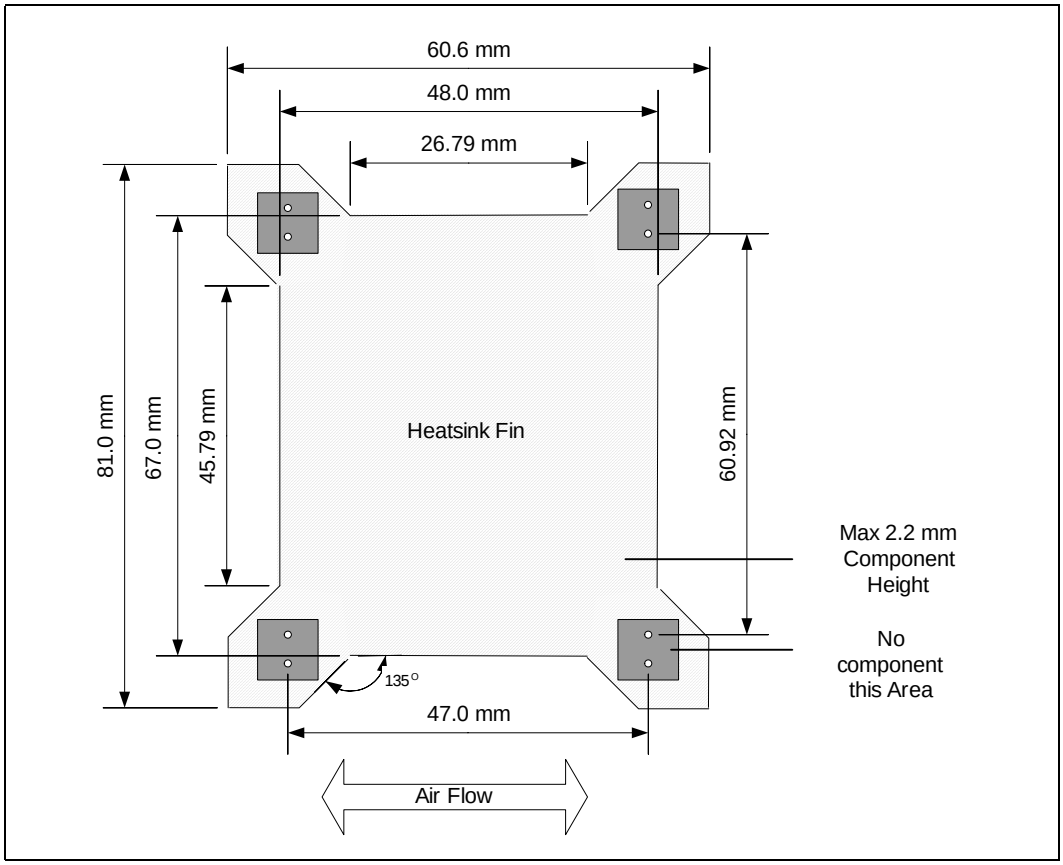
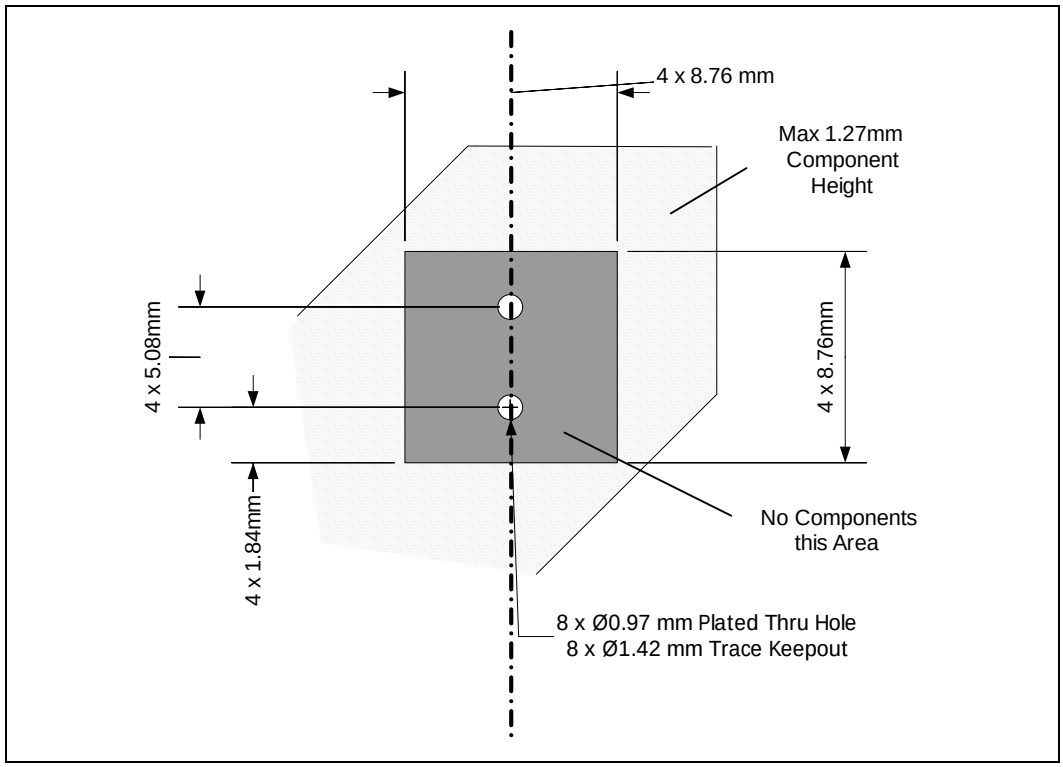


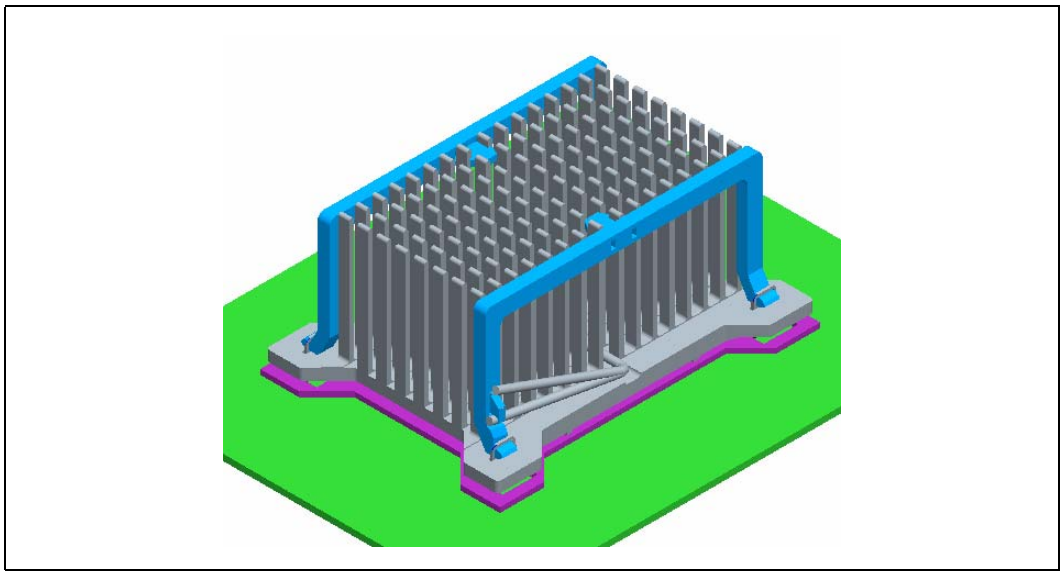
Figure 6-4. Retention Mechanism Component Keepout Zones



6.5.1 Heatsink Orientation

Since this solution is based on a unidirectional heatsink, mean airflow direction must be aligned with the direction of the heatsink fins.

Figure 6-5. Plastic Wave Soldering Heatsink Assembly



6.5.2 Extruded Heatsink Profiles

The reference thermal solution uses an extruded heatsink for cooling the chipset MCH. Figure 6-6 shows the heatsink profile. Appendix A lists a supplier for this extruded heatsink. Other heatsinks with similar dimensions and increased thermal performance may be available. Full mechanical drawing of this heatsink is provided in Appendix B.

6.5.3 Mechanical Interface Material

There is no mechanical interface material associated with this reference solution.

6.5.4 Thermal Interface Material

A thermal interface material (TIM) provides improved conductivity between the die and heatsink. The reference thermal solution uses Chomerics T-710*, 0.127 mm (0.005 in.) thick, 15 mm x 15 mm (0.60 in. x 0.60 in.) square.

Note: Unflowed or “dry” Chomerics T710 has a material thickness of 0.005 inch. The flowed or “wet” Chomerics T710 has a material thickness of ~0.0025 inch after it reaches its phase change temperature.

6.5.4.1 Effect of Pressure on TIM Performance

As mechanical pressure increases on the TIM, the thermal resistance of the TIM decreases. This phenomenon is due to the decrease of the bond line thickness (BLT). BLT is the final settled thickness of the thermal interface material after installation of heatsink. The effect of pressure on the thermal resistance of the Chomerics T710 TIM is shown in Table 6-1. The heatsink clip provides enough pressure for the TIM to achieve a thermal conductivity of 0.17°C $inch^2$/W.

Table 6-1. Chomerics T710 TIM Performance as a Function of Attach Pressure

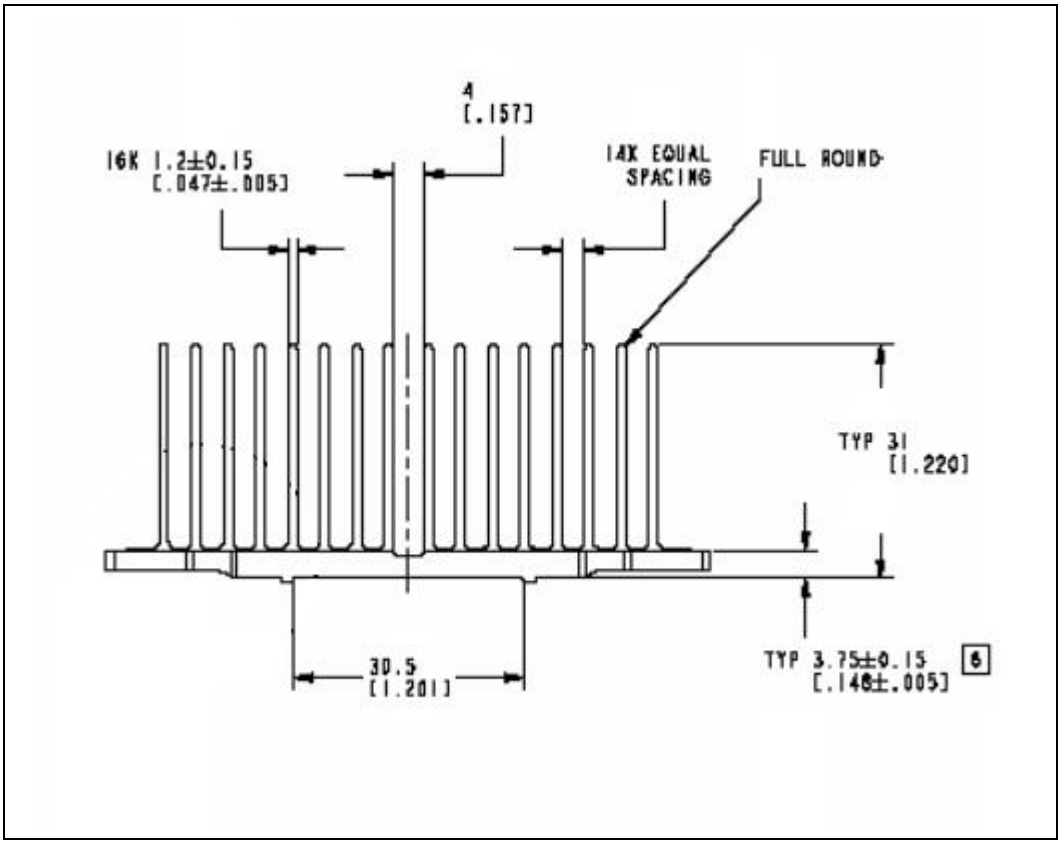
Pressure (psi)	Thermal Resistance (°C × in²)/W
5	0.37
10	0.30
20	0.21
30	0.17

NOTE: All measured at 50°C.

6.5.5 Heatsink Clips

The retention mechanism in this reference solution includes two different types of clips, one is ramp clip and the other is wire clip. Each end of the wire clip is attached to the ramp clip which in turn attaches themselves to anchors to fasten the overall heatsink assembly to the motherboard. See Appendix B for a mechanical drawing of the clip.

Figure 6-6. Plastic Wave Soldering Heatsink Extrusion Profile



6.5.6 Clip Retention Anchors

For Intel E7230 chipset-based platforms that have very limited board space, a clip retention anchor has been developed to minimize the impact of clip retention on the board. It is based on a standard two-pin jumper and is soldered to the board like any common through-hole header. A new anchor design is available with 45° bent leads to increase the anchor attach reliability over time. See Appendix A for the part number and supplier information.

6.6 Reliability Guidelines

Each motherboard, heatsink and attach combination may vary the mechanical loading of the component. Based on the end user environment, the user should define the appropriate reliability test criteria and carefully evaluate the completed assembly prior to use in high volume. Some general recommendations are shown in Table 6-2.

Table 6-2. Reliability Guidelines

Test (1)	Requirement	Pass/Fail Criteria (2)
Mechanical Shock	50 g, board level, 11 msec, 3 shocks/axis	Visual Check and Electrical Functional Test
Random Vibration	7.3 g, board level, 45 min/axis, 50 Hz to 2000 Hz	Visual Check and Electrical Functional Test
Temperature Life	85°C, 2000 hours total, checkpoints at 168, 500, 1000, and 2000 hours	Visual Check
Thermal Cycling	–5°C to +70°C, 500 cycles	Visual Check
Humidity	85% relative humidity, 55°C, 1000 hours	Visual Check

NOTES:
1. It is recommended that the above tests be performed on a sample size of at least twelve assemblies from three lots of material.
2. Additional pass/fail criteria may be added at the discretion of the user.

§

A Thermal Solution Component Suppliers

A.1 Plastic Wave Soldering Heatsink Thermal Solution

Part	Intel Part Number	Supplier (Part Number)	Contact Information
Heatsink Assembly includes: • Unidirectional Pin-Fin Heatsink • Thermal Interface Material • Ramp Clip • Wire Clip	C92237-001	CCI	Monica Chih (Taiwan) 866-2-29952666, x131 monica_chih@ccic.com.tw Harry Lin (CCI/ACK-USA) 714-739-5797 hlinack@aol.com
Undirectional Pin-Fin Heatsink (42.30 x 42.30 x 29.0 mm)	C92139-001	CCI	Monica Chih (Taiwan) 866-2-29952666, x131 monica_chih@ccic.com.tw Harry Lin (CCI/ACK-USA) 714-739-5797 hlinack@aol.com
Thermal Interface (T710)	-	Chomerics	Todd Sousa (USA) 360-606-8171 tsousa@parker.com
Heatsink Ramp Clip	C92140-001	CCI	Monica Chih (Taiwan) 866-2-29952666, x131 monica_chih@ccic.com.tw Harry Lin (CCI/ACK-USA) 714-739-5797 hlinack@aol.com
Heatsink Wire Clip	C85373-001	CCI	Monica Chih (Taiwan) 866-2-29952666, x131 monica_chih@ccic.com.tw Harry Lin (CCI/ACK-USA) 714-739-5797 hlinack@aol.com

Part	Intel Part Number	Supplier (Part Number)	Contact Information
Solder-Down Anchor	C85376-001	Wieson	Rick Lin Deputy Manager/Project Sales Department Add.: 7F, No. 276, Section 1, Tatung Road, Hsichih City, Taipei Hsien, Taiwan Tel: 886-2-2647-1896 ext. 6342 Mobile: 886-955644008 Email: rick@wieson.com Website: www.wieson.com

Note: The enabled components may not be currently available from all suppliers. Contact the supplier directly to verify time of component availability.

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B Mechanical Drawings

Table B-1 lists the mechanical drawings included in this appendix.

Table B-1. Mechanical Drawing List

Drawing Description	Figure Number
Plastic Wave Soldering Heatsink Assembly Drawing	Figure B-1
Plastic Wave Soldering Heatsink Drawing (1 of 2)	Figure B-2
Plastic Wave Soldering Heatsink Drawing (2 of 2)	Figure B-3
Plastic Wave Soldering Heatsink Ramp Clip Drawing (1 of 2)	Figure B-4
Plastic Wave Soldering Heatsink Ramp Clip Drawing (2 of 2)	Figure B-5
Plastic Wave Soldering Heatsink Wire Clip Drawing	Figure B-6
Plastic Wave Soldering Heatsink Solder-down Anchor Drawing	Figure B-7

Figure B-1. Plastic Wave Soldering Heatsink Assembly Drawing

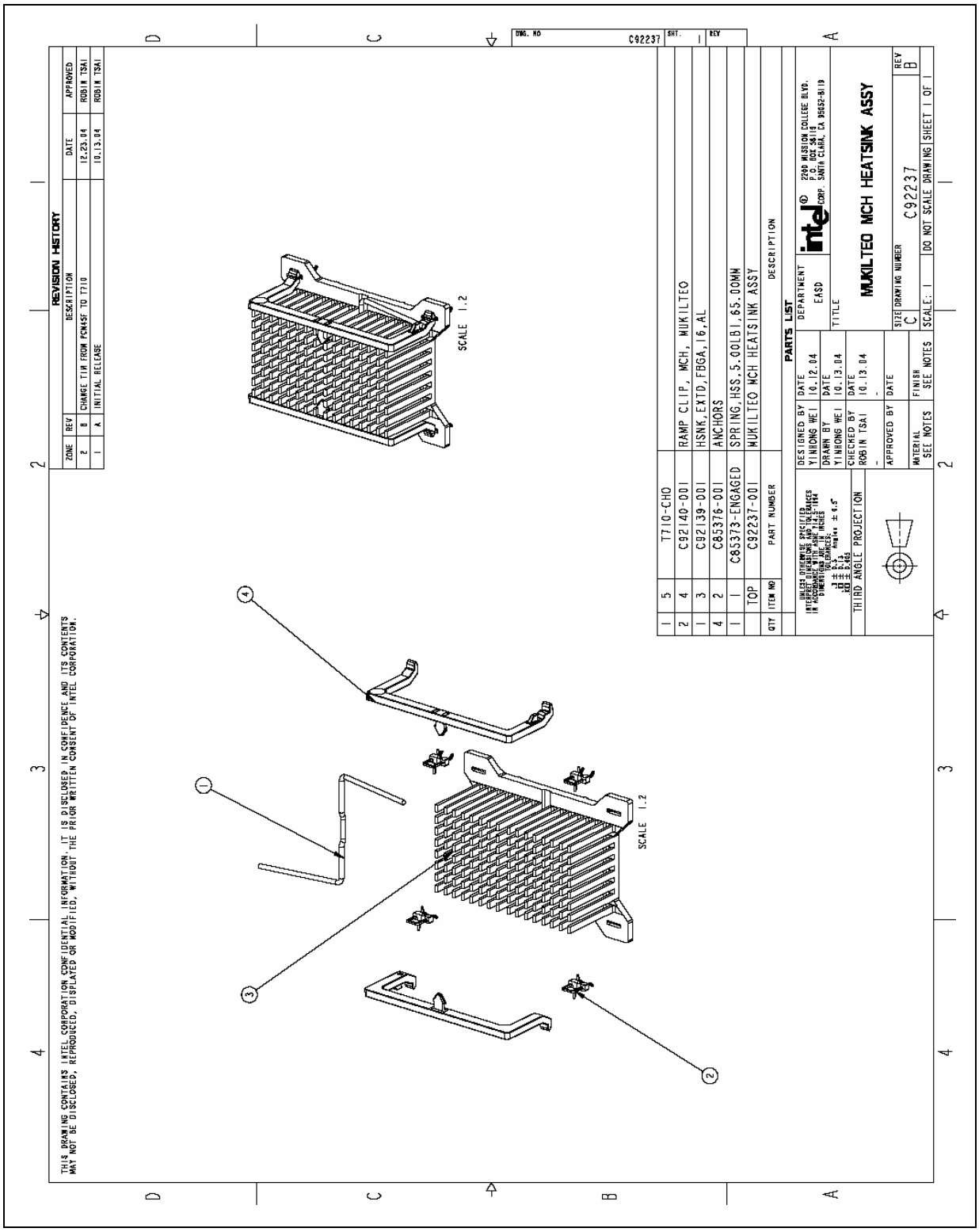


Figure B-2. Plastic Wave Soldering Heatsink Drawing (1 of 2)

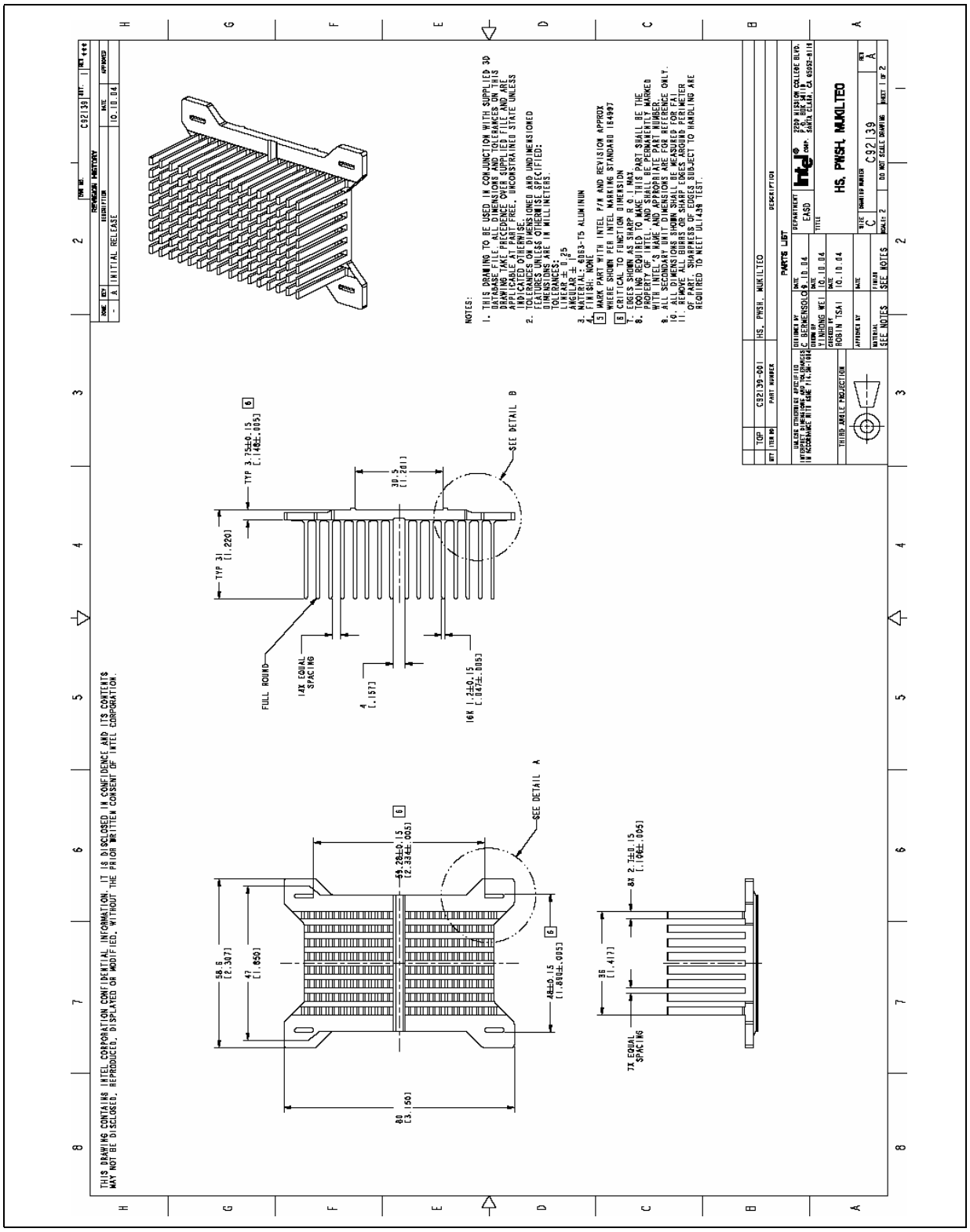


Figure B-3. Plastic Wave Soldering Heatsink Drawing (2 of 2)

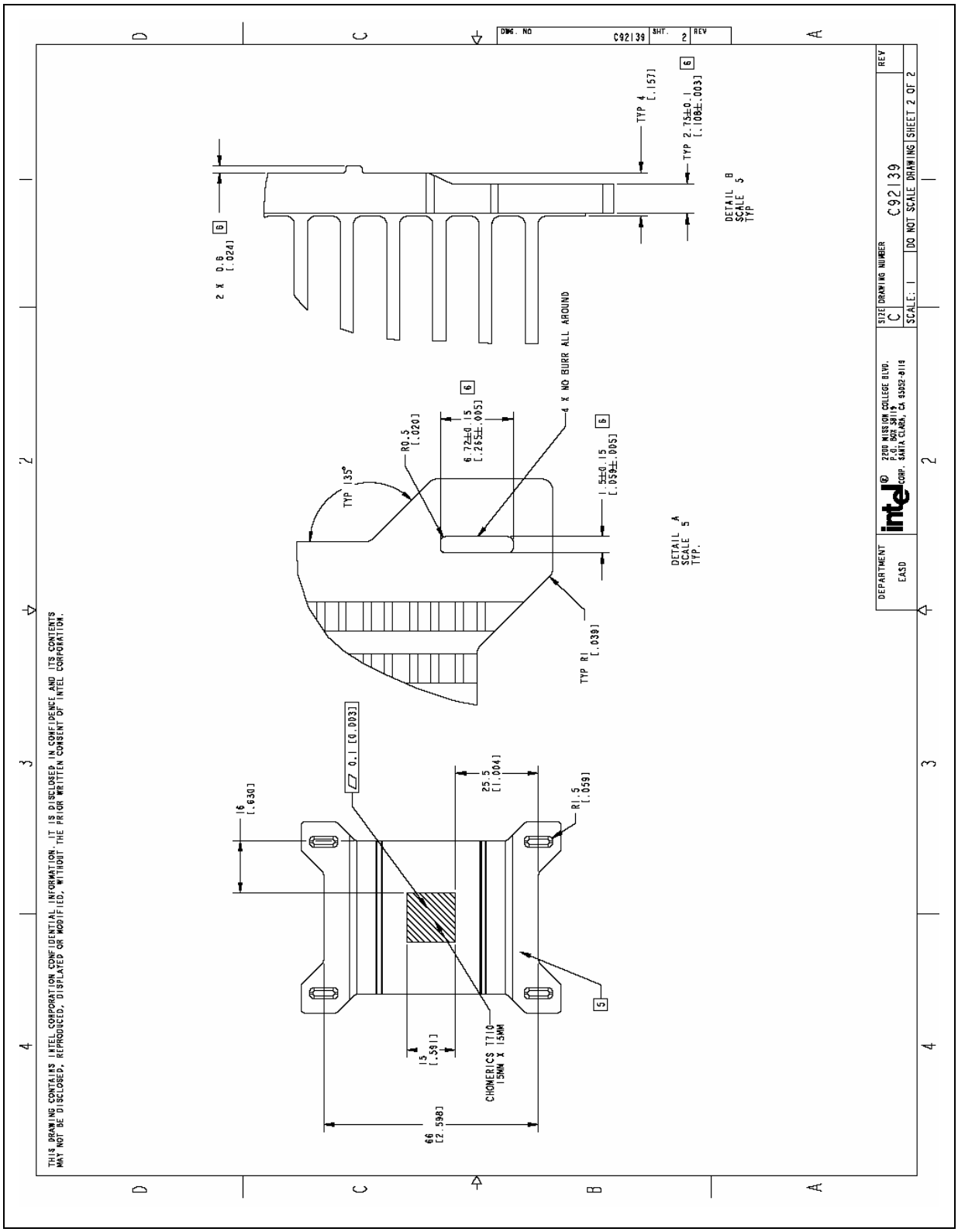


Figure B-4. Plastic Wave Soldering Heatsink Ramp Clip Drawing (1 of 2)

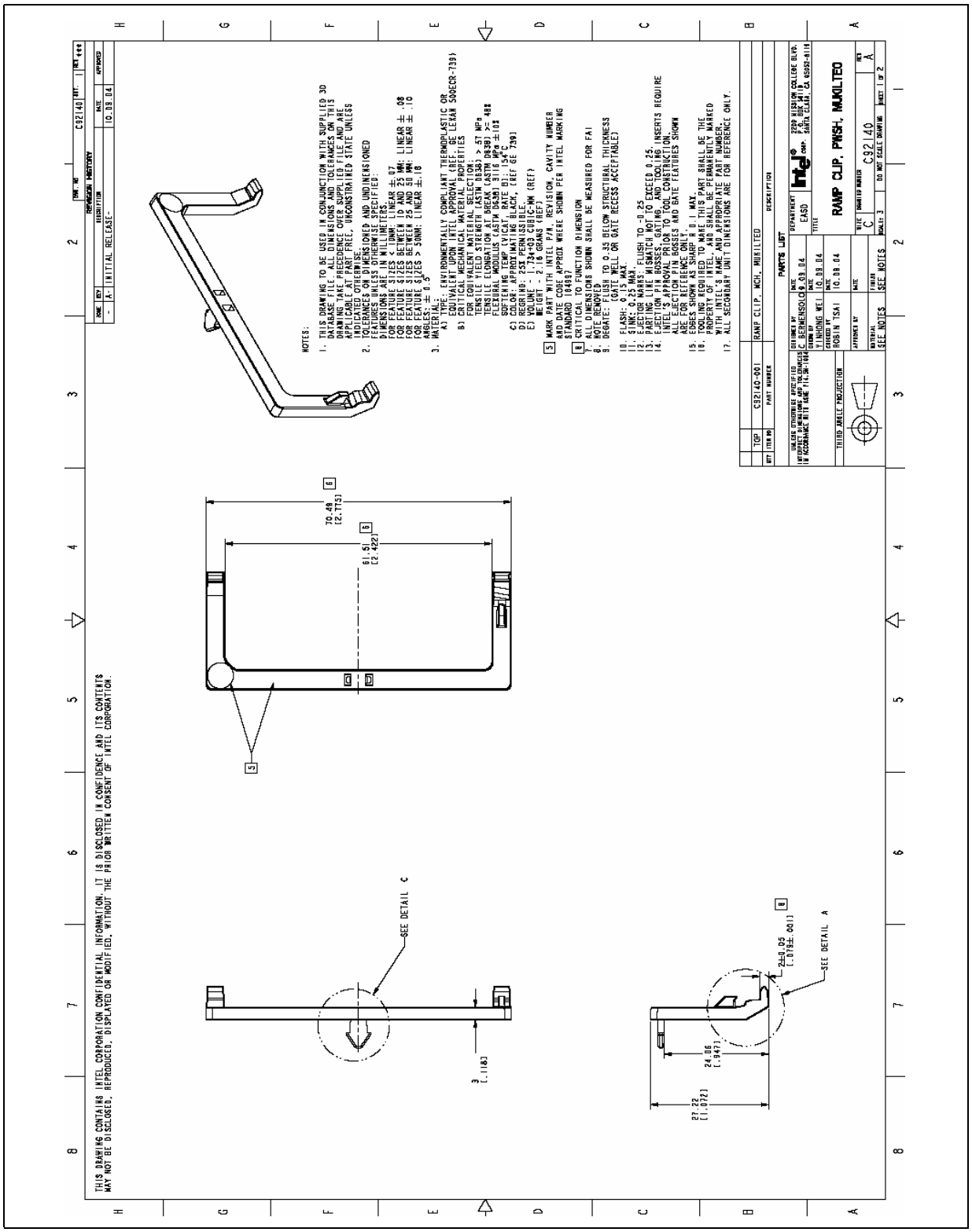


Figure B-5. Plastic Wave Soldering Heatsink Ramp Clip Drawing (2 of 2)

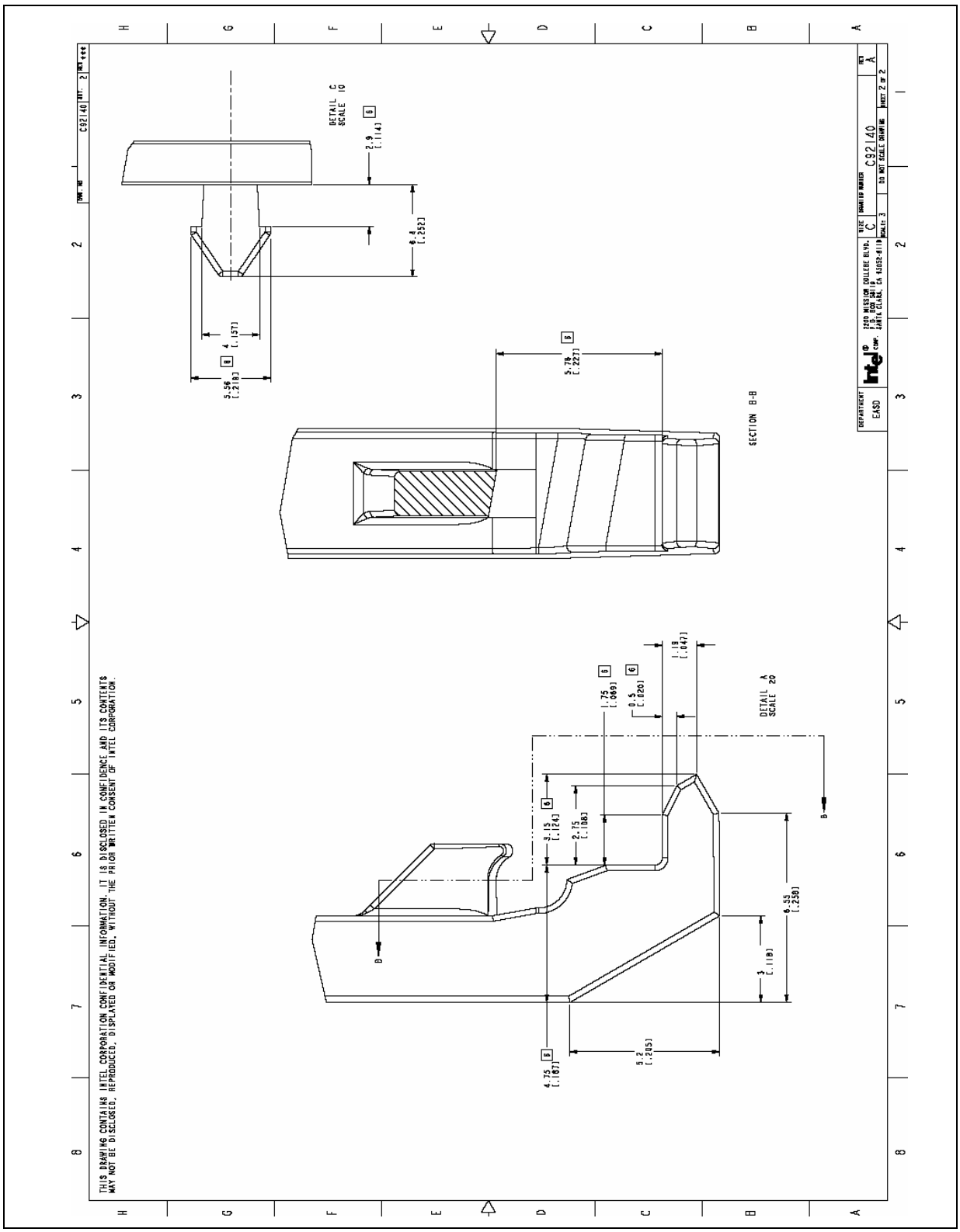


Figure B-6. Plastic Wave Soldering Heatsink Wire Clip Drawing

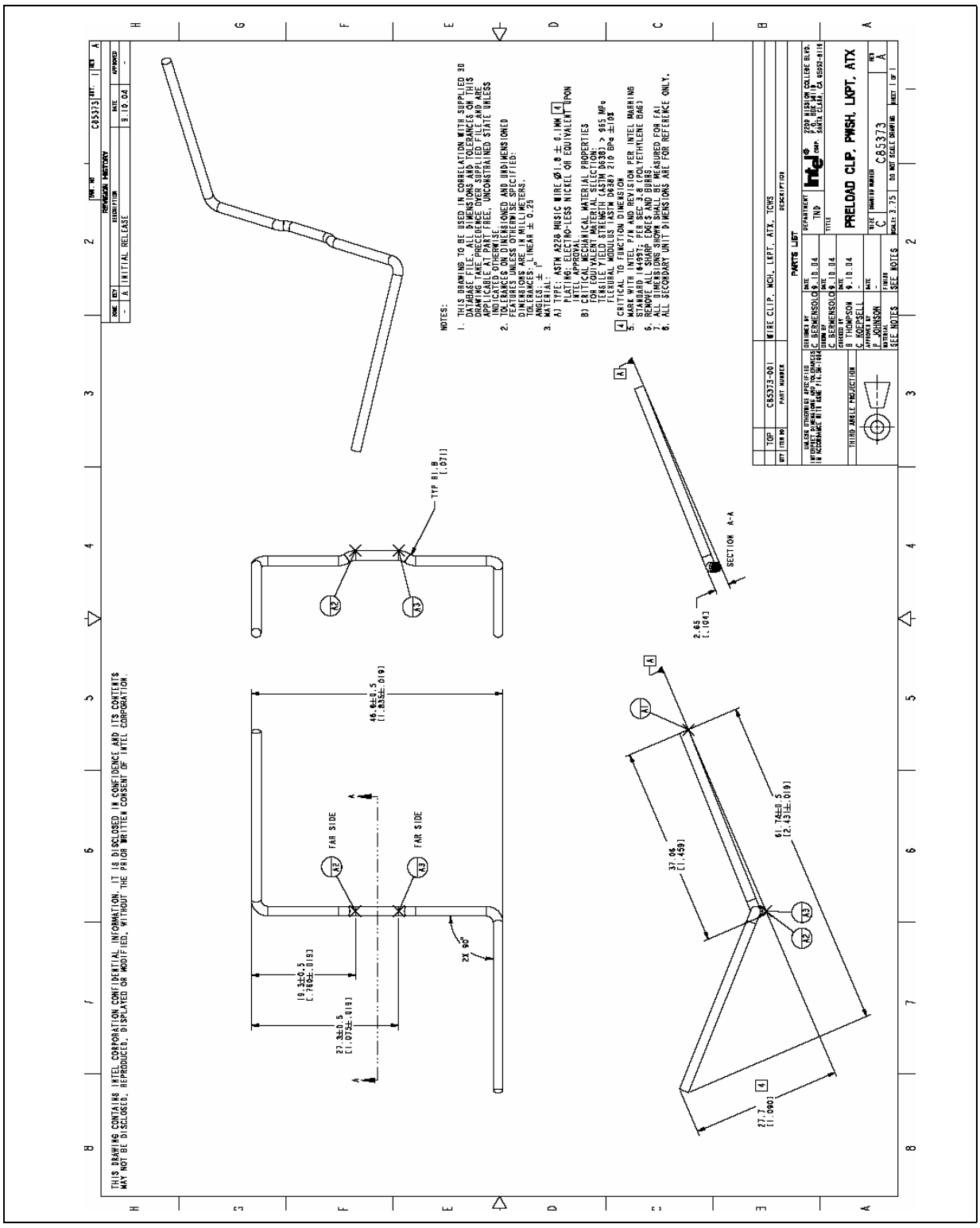
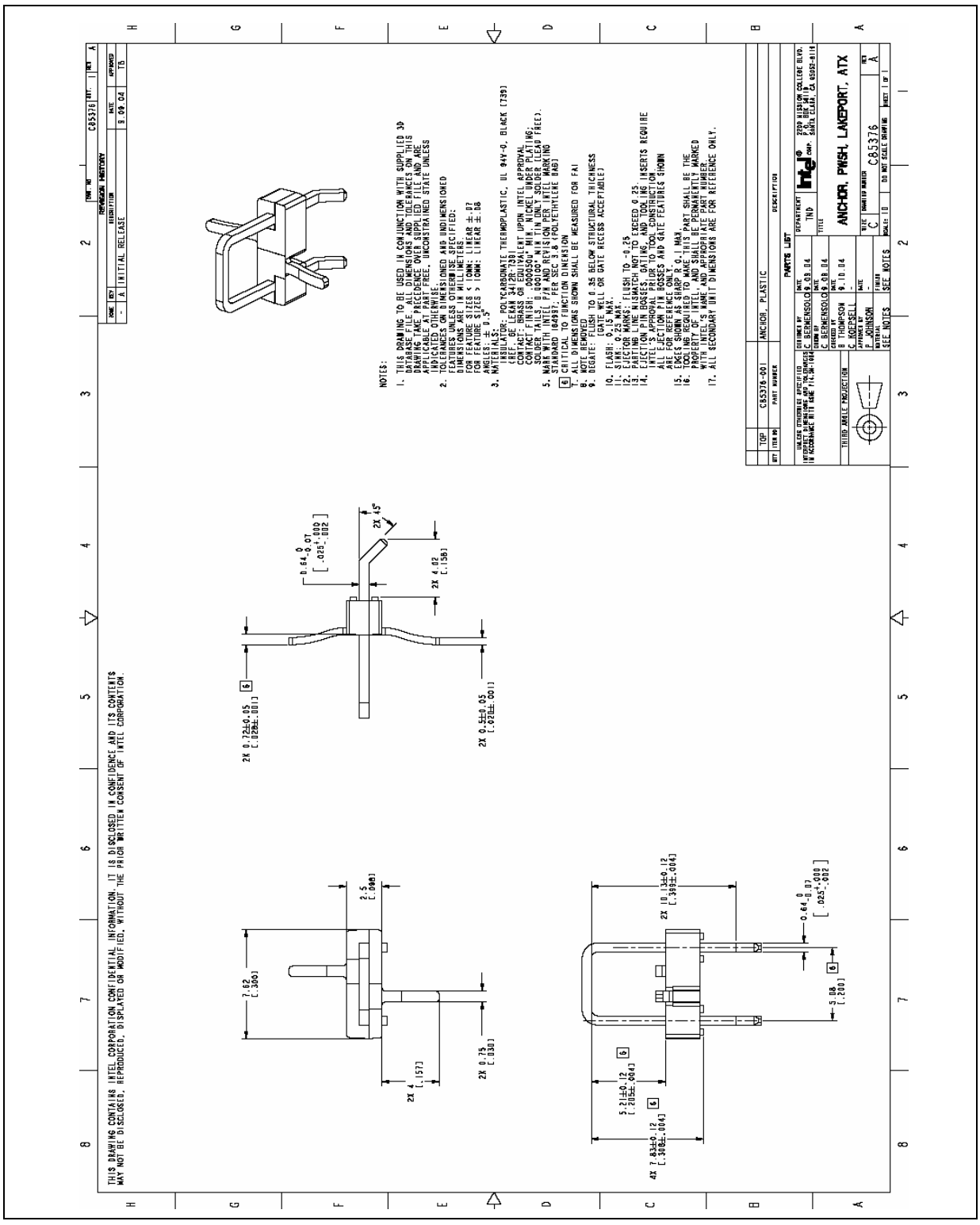


Figure B-7. Plastic Wave Soldering Heatsink Solder-down Anchor Drawing



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